TC11 Student Competition: Fault-Tolerant Power Converter for Aerospace

Topic

Fault-Tolerant Converter Design for Aerospace Applications

Participants are invited to design a fault-tolerant unidirectional DC-DC power converter for aerospace applications. The converter type is open-topic: participants may design DC-DC, DC-AC, AC-DC converters, motor drives, or other relevant circuits.

Aerospace systems demand unparalleled reliability, and this challenge emphasises true fault tolerance — elimination of single points of failure (SPOF). The converter should continue operating seamlessly even if any single component fails, with only minimal and temporary performance degradation permitted during fault transition.

Designs should be suitable for a broad range of aerospace applications (e.g., aircraft, spacecraft, satellites), provided they meet the required electrical specifications.

Both simulation-based and hardware-prototype solutions are welcome. Submissions must include verification results to demonstrate performance under both nominal and fault conditions. Hardware demonstrations are encouraged but not mandatory.

Background and Motivation

The Critical Role of Fault Tolerance in Aerospace Power Systems

In aerospace environments, electronic systems are subjected to extreme conditions, including temperature fluctuations, radiation, and potential physical damage from micrometeoroids. For instance, a power converter aboard a spacecraft might suffer structural damage due to micrometeoroid impacts, potentially destroying parts of the circuit. If the converter continues to operate despite such damage, it significantly enhances the spacecraft's survivability and mission success.

Traditional power converter designs often contain single points of failure, which can lead to catastrophic outcomes in aerospace applications. Therefore, developing fault-tolerant power converters—capable of maintaining operation despite individual component failures—is paramount for ensuring safety and reliability in these critical systems.

Advancing Innovation in Power Electronics

While fault-tolerant designs are gaining attention, they are not yet widely adopted in aerospace power electronics. This competition aims to bridge that gap by challenging participants to innovate beyond conventional designs.

Alignment with Industry Standards

Designs developed for this competition should consider compliance with industry standards like RTCA DO-160 and MIL-STD-461, which outline environmental and electromagnetic compatibility requirements for aerospace equipment. Adhering to these standards ensures that the proposed solutions are not only innovative but also practical and applicable to real-world aerospace systems.

Objectives of the Competition

The competition is designed to serve multiple objectives that benefit both academia and industry in the field of power electronics:

Advance the State of the Art: By tackling the rarely addressed challenge of fault tolerance in aerospace power converters, the competition encourages participants to push beyond conventional design practices and propose genuinely novel architectures.

Promote Education Through Application: The challenge combines deep theoretical insight with practical implementation. Participants are expected to back their designs with solid analysis—demonstrating not only that the converter works, but why and how it remains stable and coordinated under fault conditions.

Bridge Academia and Industry: The competition aims to foster collaboration between universities and aerospace power industry leaders. With participation from industry judges and potential sponsors, the event offers students a platform to showcase their ideas to influential figures in the field.

Encourage Practical Innovation: While grounded in rigorous academic principles, the designs should ultimately be implementable in real-world systems. Solutions that demonstrate operational viability, modularity, and scalability will be especially encouraged.

Eligibility and Team Composition

The competition is open to all students, including PhD, Master's, and undergraduate students, from universities and research institutions worldwide. Teams may consist of up to 3 members. Teams can be **interdisciplinary**, encouraging collaboration across different fields (e.g., power electronics, control systems, aerospace engineering). Additionally, **cross-institutional teams** are allowed, promoting collaboration between

universities and fostering a diverse exchange of ideas. The competition welcomes international collaborations.

Submission Guidelines

Multi-phase Submission Process:

Phase 1: Expression of Interest (EoI)

- A brief design form describing the fault-tolerant converter architecture and theoretical justification for fault tolerance.

Phase 2: Report Submission

- A comprehensive technical report (maximum 35 pages, A4 or US Letter format), including:
    - Design methodology
    - Theoretical analysis and control strategy
    - Fault injection scenarios and mitigation response
    - Simulation results (and optional hardware implementation)
    - Discussion on aerospace applicability and compliance with relevant standards
    - BOM and cost
- Hardware demonstration videos are encouraged to showcase functionality and fault recovery, but are not mandatory.

Phase 3: Finalist Presentations

- Shortlisted teams will be invited to deliver a virtual (online) presentation to a panel of academic and industry experts.
- Presentations will include Q&A to evaluate technical depth, clarity, and originality.

Templates

Design report and proposal templates will be provided to ensure consistency across submissions.

Timeline

Milestone	Date
Competition Launch & Info Session	ECCE 2025
EoI Submission Deadline	30 November 2025
Report Submission Deadline	15 January 2026
Presentations	February 2026
Awards	APEC 2026

Rules and Specifications

Fault Tolerance:

- Minimizing the number of single point of failures (SPOFs).
- The system should continue operating under any single component failure, including but not limited to:

  - Power switches (MOSFETs/IGBTs)
  - Gate drivers
  - Control circuits (controllers, sensors)
  - Passive components (capacitors, inductors, transformers, resistors)
  - Optocouplers
  - Power sources (partial or complete input module fault)
  - PCB tracks

- Transient disturbances are acceptable, but the converter must restore functionality rapidly and stably without user intervention.
- Teams must demonstrate and justify how their design achieves fault tolerance, with both theoretical analysis and simulated (or experimental) fault injections.

Design Flexibility:

- Converter topology is open-ended. Any architecture may be proposed (modular, redundant, multilevel, etc.).
- Teams may use any control strategy, including decentralized, distributed, or hybrid approaches, as long as they justify stability and reliability.
- No restrictions on component choice (e.g., silicon, SiC, GaN devices) or control platforms.

Verification:

- All designs must be verified through detailed simulations (MATLAB/Simulink, PLECS, LTSPICE, or equivalent).
- Hardware prototypes are optional, but strongly encouraged and will positively impact evaluation.
- Fault scenarios must be included in the verification and demonstrate continued operation.

Other Rules:
- Teams must not exceed 3 members.
- Each team must submit original work. Plagiarism or reuse of existing published designs without citation will result in disqualification.
- Each team shall submit only one entry.
- Assistance from advisors is allowed, but the core design and documentation must be student-led.

Evaluation Criteria

Criteria	Weight (%)	Details
Fault Tolerance and Reliability	30%	Effectiveness in eliminating single points of failure and handling real-world fault scenarios. Quality of analysis and validation of continued operation under failure.
Innovation and Design Creativity	20%	Novelty in converter topology, control strategy, redundancy, or fault-handling mechanism. Use of unconventional ideas with practical impact.
Technical Soundness	20%	Rigor of theoretical justification, stability analysis, and engineering feasibility. Clarity in assumptions and design trade-offs.
Verification and Demonstration	15%	Quality of simulation or hardware demonstration. Realism of fault injection scenarios and accuracy of results.
Aerospace Applicability	10%	Suitability of the design for aerospace environments (e.g., compliance with DO-160/MIL-STD principles, modularity, weight, reliability).
Presentation and Communication	5%	Clarity, completeness, and professionalism of the final report and oral presentation. Ability to convey design rationale effectively.

Prize

Awards:
- 1x First Prize: Cash ($5k), Certificate
- 1x Second Prize: Cash ($3k), Certificate
- 2x Third Prize: Cash ($1k), Certificate

Additional Recognition:
- Selected top entries may be featured in IEEE Power Electronics Society (PELS) publications or invited for short presentations at major conferences (subject to collaboration with sponsors).
- All shortlisted teams will receive digital certificates and may be offered networking opportunities with academic and industry partners.

Note: Further sponsor information will be announced at a later stage. Interested organizations are welcome to inquire about sponsorship opportunities.