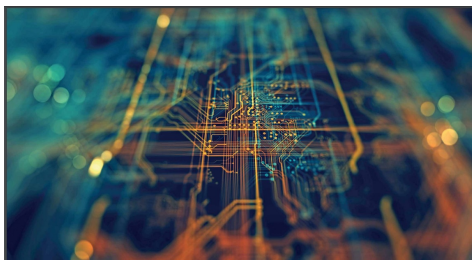


## IEEE Power Electronics Magazine



Printed circuit board (PCB) layout has been an integral aspect of power electronic design since the first switching power supplies appeared more than 40 years ago. Regardless of the transistor technology, the parasitic impedances added to the circuit by the PCB layout must be understood and managed for the circuit to function correctly, reliably, and without causing undue electromagnetic interference (EMI). In the June 2023 issue of *IEEE Power Electronics Magazine*, the article “**Optimizing PCB Layout for HV GaN Power Transistors**,” by Eric

Persson, discusses several key concepts to help understand the layout challenges and strategies needed to solve these challenges and optimize the layout for best overall electrical and thermal performance. Read these “Tips” starting on page 65 of the June issue.

### Free for All

Visit the magazine [website](#) for various open access columns and society news stories.

## IEEE Transactions on Power Electronics (TPEL)

TPEL has several announcements for the month of August.

### ① Call for Proposals in TPEL Special Sections

*IEEE Transactions on Power Electronics* (TPEL) is seeking multiple proposals for special sections to be published in 2024. There are 2 required documents: [Call for Proposals](#) and the [Guest Editorial Board Information](#) spreadsheet. The deadline for CFP is August 31, 2023. Proposals for the TPEL special sections should be emailed to the TPEL [EIC](#) and the TPEL [Admin](#). For more information, contact the TPEL Admin: [marybeth.schwartz@ieee.org](mailto:marybeth.schwartz@ieee.org).

### ② The September 2023 issue of TPEL is now available [online](#). Be sure to check out these highlighted articles selected by TPEL editors.

“**Active Peltier Effect Heat Sink for Power Semiconductor Device Thermal Stability Enhancement**,” by Lijian Ding, Ruya Song, Shuang Zhao, Jianing Wang, and Homer Alan Mantooth. The paper proposes a Peltier effect heat sink (PEHS) to dynamically manage thermal stress in power semiconductor devices, significantly reducing temperature fluctuations and enhancing their long-term reliability.

“**ConverGenT: Automated Topology Generation and Analysis of Hybrid DC–DC Converters**,” by Huan Nguyen and Wanyong Jung. The paper presents an automated system for generating and analyzing hybrid dc–dc converter topologies, identifying 62 superior converter families and enhancing efficiency over traditional methods.

③ Starting September 1, 2023, there will be a change in the submission requirements for TPEL. This measure is to protect our authors. It will be mandatory that all submissions have a primary email address that is institutional. Examples of institutional emails include those from an academic institution, a government agency, a company, or IEEE. Papers that do not meet this requirement will not be entered into the review process. We thank you for your assistance with this submission update.

## IEEE Power Electronics Letters

TPEL Letters has a few news items to share for August.

### ① We will soon be announcing a new Letters Special Section, with a Call for Papers starting in September.

② In the **August 2023** issue of TPEL, we have 12 Letters published which include novel model of common-mode inductor, new packaging and condition monitoring methods for wide-bandgap devices, novel converter circuits and control methods, advancements in motor drives, hardware-in-the-loop simulation algorithms, simultaneous wireless power and data transfer systems, and radio-frequency power amplifiers. Two intriguing Letters from the issue are highlighted below.

“**High Performance SiC Power Module Based on Repackaging of Discrete SiC Devices**,” by Zibo Chen and Alex Q. Huang. This work demonstrates a cost-effective way to repackage discrete SiC devices as high-current power modules. The repackaged SiC power module features over 50 percent cost reduction and demonstrates excellent electrical and thermal performance. A 75 kW two-stage dc-dc/dc-ac converter is built to validate the performance of a repackaged six-phase SiC power module.

“**Predicting Common-Mode Inductor Current Using a Time-Domain Hysteresis Model**,” by Harshita Singh and Scott D. Sudhoff. This work highlights the significant impact of magnetic hysteresis and parasitic capacitance in the design of common-mode inductor. Considering the impact, an enhanced model of common-mode inductor that can more accurately predict the common-mode current is developed and validated in experiments.

## IEEE Open Journal of Power Electronics (OJPEL)

OJPEL currently has three active Calls for Papers! Take a look below to see if a paper you are currently working on may fit with one of them. (Note that PELS members also get a publishing discount.)

- ① **Wide Bandgap Devices for Next-Generation Automotive Applications** (Deadline: August 15)
- ② **Advancement on Experimental Testing Laboratories and Measurement Systems for Power and Energy Systems** (Deadline: October 1)
- ③ **2023 IEEE 8th Electronic Grid Workshop (eGrid 2023)** (Deadline: January 1, 2024)

For more information, please visit our [website](#).

## IEEE Transactions on Transportation Electrification (TTE)

The editorial team of *IEEE Transactions on Transportation Electrification (TTE)* is pleased to announce a **Call for Papers: Special Issue on Electrified Ship Technologies**. The full paper submission deadline is January 31, 2024. The expected publication date is September 2024. All manuscripts must be submitted through [Manuscript Central](#).

## IEEE Journal of Emerging and Selected Topics in Power Electronics (JESTPE)

Are you currently working on a paper that includes new results in the field of power electronics? Consider publishing your work in JESTPE. It is a bi-monthly publication that has a review turnaround time of 2 to 3 months. JESTPE also organizes different special issues throughout the year. More information about publishing with JESTPE can be found [here](#).



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